On Silicon On Insulator Technology and Devices

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This article describes the silicon on insulator technologies (SOI) and devices. Different methods of forming SOI wafers are presented and advantages and weakness of the massive silicon technology is reviewed. SOI-MOSFET related physical and electrical phenomena, as well as some innovating architectures is presented.

1. Presentation of SOI technologies

Massive silicon is the material on which microelectronics is based. In the MOS technology carried out on massive silicon, only a finite part close to the interface is used for electrical conduction and the remainder is without utility. On the other hand, in SOI technologies a silicon film is carried by a more or less thick insulating layer under which the silicon wafer is located. The SOI material is thus only one stacking of three layers as shown in Fig. 1.

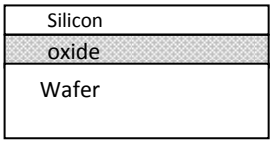

Fig.1.

The SOI wafers have the same characteristics as those that were made on massive silicon and as a result they can be treated by the same equipment. This why there much interest in such a technology.

2. Methods of forming SOI wafers

SOI technologies can be divided into two groups. In the first group, the silicon film is deposited directly onto an insulating substrate, which is the case of silicon on sapphire (SOS) and silicon on zirconia (SOZ). In the second group, a thin insulating layer is used to separate the active semiconductor layer from the semiconductor substrate (SIS). Methods of forming SOI wafers include separation by oxygen implantation (SIMOX), zone melting re-crystallization (ZMR) of poly-silicon, epitaxial lateral overgrowth (ELO), full isolation by porous oxidized silicon (FIPOS), and wafer bonding (WB).

2.1. Standard SIMOX

Among the SOI technologies, SIMOX is considered to be the most advanced and promising for high density CMOS circuits. The buried layer of silicon is carried out by direct implantation of oxygen in the silicon wafer with a large amount ($1.8\ 10^{18}\ O^{+}\ Cm^{-1}$) and energies (200keV), once the implantation is completed, we subject the structure to an annealing at high temperature HTA 1320°C for six hours that has a double role, the elimination of the precipitates and residual defects and the creation of abrupt interface [1, 2]. This process allows having layer with thickness closer 40 nm (Fig. 2).

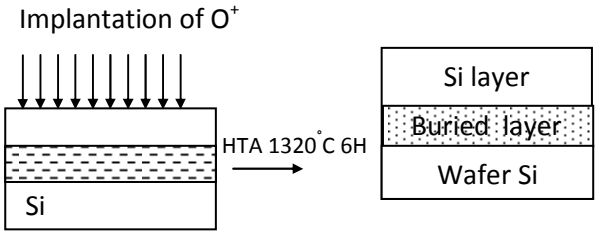

Fig.2: Standard SIMOX.

3. Advantages of SOI technology

1) Ionizing mediums.
2) Insulation
3) Elimination of parasitic thyristor
4) Reduction of drain /source junction
5) Operating in high temperature
6) Three-dimensional integration
7) Reduction of short channel effects
8) Saturation current is high than MOS/Si transistor

9) Reduction of carriers effects
10) Reduction of substrate polarization effect.

4. SOI MOS transistor

The SOI-MOSFET obeys the same operational principle as massive silicon MOSFET. However, the difference is that conduction can be controlled by two gates, called the front and the back gate, which creates for each one a zone of space charge. According to the relationship between the thickness of silicon film and the width of the two depletion zones, the SOI-MOSFET can be divided into two groups, partially depleted and fully depleted. When the silicon film is very thin and only the action of one gate is sufficient to deplete completely the film, we say that we are in the fully depleted transistor

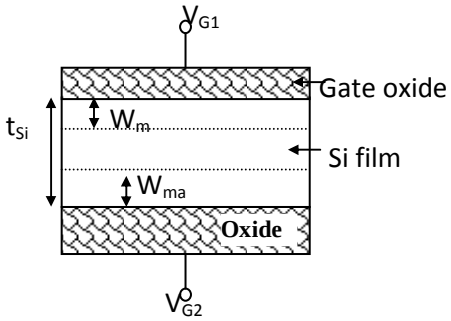

Fig.3: Zones of space charges in SOI structure.

If the silicon film is thick, the two depletion zones are independent then there exists a neutral zone. Thus, there exists a strong resemblance between massive MOSFET and SOI- MOSFET.

5. The SOI-MOFET parasitic effects

Contrary to massive silicon transistor, the SOI technology has potential for a floating substrate that is not fixed to the mass and the silicon film is completely isolated from the substrate via buried oxide. Consequently, the charges eliminated due to contact with the substrate are accumulated by neutral area, leading to a variation of the body potential and the threshold tension. The body is regarded as an additional node.

5.1. Kink effect

The kink effect denotes an abrupt increase in the saturation current of the partially depleted SOI-MOSFET working in strong inversion [3]

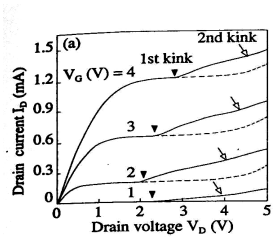

Fig.4: Experimental characteristic ID (VD) of SOI-MOSFET showing the Kink effect.

In the saturation area, the channel carriers generate pairs (electron/hole) through impact ionisation closer to the drain, the minority carriers are collected by the drain, whereas the majority carriers cross the source and give rise to the gradual charge stored in the substrate. Concomitant increase in substrate potential induces a lowering of threshold tension (V_T) and source potential barrier. Due to this reason much of the minority carriers will be able to diffuse source towards the channel. This is positive feedback.

A sudden increase induces in the drain current a phenomenon called the kink effect. The Kink is the most important effect in the SOI-MOSFET, therefore, there exist other parasitic effects, and we can quote:

1) Action of the paratactic bipolar transistor
2) Transient phenomena
3) Edge effect
4) Self heating effect

6. Innovating architectures

Many innovating architectures were proposed, we distinguish:

1) The DTMOSFET
2) The double gate SOI-MOSFET
3) The ground plan SOI-MOSFET

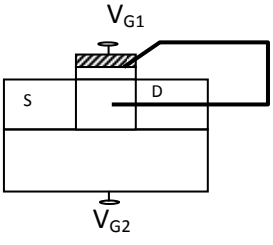

Fig.5: DTMOSFET.

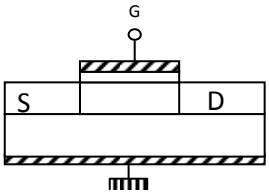

Fig.6: Ground plan MOSFET

7. Conclusion

SOI offers the advisability of integrating devices, presenting high performances and/or of innovating elements to push back the limits of CMOS technology. The SOI technology is a substitution solution for the massive silicon technology. It makes it possible to rise above the constraints felt in the massive silicon technology and gives a second breath to microelectronics, if its weaknesses find technological solutions.

References

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[3] Thomas Ernst, ''Etude des structures MOSFET avancées sur SOI pour les applications basse consommation'', Thèse INPG (2000).