

A Simple FPGA-Based Lossless Wireless Transmitter/Receiver Using the Residue Number System

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1. Introduction

Wireless system design often feature FPGAs alongside DSPs and FPGAs, which offer superior speed compared to other processors and operate close to the antenna and are the core of a larger processor in the transmitter and receiver blocks.

In the transmitter, a methodology to analyze factored orthogonal 1-D DWT based on the wavelet lifting scheme and the RNS is used. The wavelet lifting scheme is used because it allows an in-place implementation and reduces the forward transform to a sequence of simple steps involving elementary algebraic operations that make it trivial to find the inverse transform [1, 2].

However, scaling is inherent in all lifting transforms and does not yield integer results. Many methods exist to overcome this scaling [3]. However, these approaches introduce further processing that can increase algorithmic complexity. To simplify system design, the scaling factor is assumed to be unity in this approach. As a result, minimization of the circuit design is enhanced while retaining system high-fidelity.

The residue digits from the RNS and wavelet lifting scheme are transformed into orthogonal signals through the mapping to a set of Walsh functions. The orthogonal signals are then multiplexed unto a carrier wave and transmitted to the receiver.

In the receiver, the low-pass equivalent composite signal made-up of the set of orthogonal signals is passed through a bank of correlators. The scalar products of the transmitted signal and stored copies of the Walsh functions are used to find the optimum estimate of the residue digits. The Chinese remainder theorem is later used to recover the message.

In the proposed communication system, the message is considered to be subjected only to quantization noise. The channel requirements and the FPGA inherent speed render effects due to additive white Gaussian noise negligible. It is shown that [4], for a quantization error, $P_e \leq 10^{-5}$

the decoding errors have negligible effect. Using this error threshold, the RMS error for different moduli set is calculated for a given test signal.

2. Main results

For simulation purposes, assume a message of $f(t) = \sin(300t) + 2 \sin(315t) + \sin(320t) + \sin(350t)$.

The RMS error for different moduli set is calculated as follows

$$\text{Error}_{\text{RMS}} = \sqrt{\left(\frac{1}{N^2}\right) \sum_N (x_{\text{output}} - x_{\text{input}})^2} \quad (1)$$

Where, x_{output} and x_{input} are the output and input data respectively and N is the number of data points.

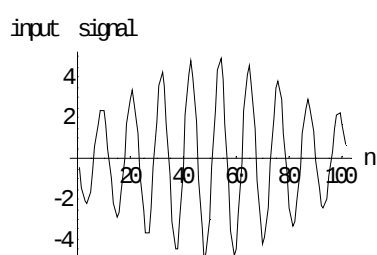
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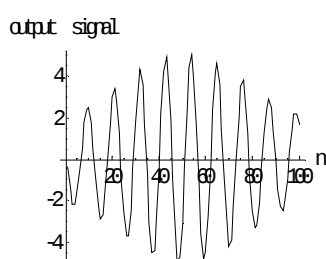
Moduli set	RMS error	Range
{11, 13, 17}	5.61188×10^{-4}	2431
{3, 5, 7}	0.105836	105
{121, 125, 127}	0.192088	1920875
{119, 125, 127}	5.8277×10^{-7}	1889125
{125, 126, 127}	5.82774×10^{-7}	2000250

From Table 1 above, it is seen that the quantization error depends on the dynamic range and the distribution of the residue sequence.

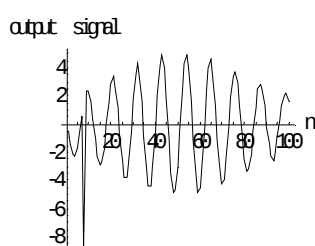
In order to verify the performance of the proposed architecture based on the residue number system and the lifting scheme, a Xilinx Virtex-4 FPGA chip (device: xc4vfx 12, package: ff1 148, speed grade-10) is used. Simulations are performed for a first-level discrete wavelet decomposition in MATLAB and ModelSim for 100 data points. Fig. 1 shows the input signal and output signal waveforms for moduli sets {125, 126, 127} and {3, 5, 7} in order to illustrate distortion with respect to error threshold value.



(a)



(b)



(c)

Fig.1: a) Input signal; b) Output signal for moduli set {125, 126, 127}; c) Output signal for moduli set {3, 5, 7}.

It is seen that for moduli set {125, 126, 127}, which corresponds to a RMS error less than the threshold value of $P_e \leq 10^{-5}$, the distortion is negligible compared to moduli set {3, 5, 7} with RMS error greater than the threshold value. The number of moduli sets shown in Table 1 is not exhaustive as many more sets could be displayed with varying values of the RMS error. For a 7-bit length moduli set, {125, 126, 127} is chosen for the lossless FPGA implementation based on the error threshold value and the criteria outlined in [5].

3. Conclusion

In this paper, an efficient architecture based on the residue number system (RNS) and the lifting scheme for a 1-D DWT has been proposed. The performance of the proposed architecture has been assessed for the 4-tap Daubechies filter bank by the implementation on Xilinx Virtex-4 FPGA chip. A

distortionless transmission over a non-fading Gaussian noise channel is attained using a 7-bit length moduli set of {125, 126, 127}. The moduli set was used to implement the first level decomposition in $N/2$ clock cycles with recombination of the detail and approximation wavelet coefficients. Future work will focus on the analysis of higher levels of decomposition and system's throughput.

References

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